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TO: Commissioner for Patents
Attn: **Examiner Jerry B. Dennison**
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FROM: George H. Gates
OUR REF.: 7603.01
TELEPHONE: (310) 642-4146

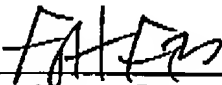
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Title of Document Transmitted:	TRANSMITTAL DOCUMENTS (2) AND REPLY BRIEF OF APPELLANTS
Applicant:	Michael G. Courts et al.
Serial No.:	09/884,523
Filed:	June 18, 2001
Group Art Unit:	2143
Title:	TRANSACTION PROCESSING SYSTEMS
Our Ref. No.:	7603.01

Please charge all fees to Deposit Account No. 14-0225 of NCR Corporation, the assignee of the present application.

By: 
Name: George H. Gates
Reg. No.: 33,500

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Due Date: November 3, 2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael G. Coutts et al.	Examiner:	Jerry B. Dennison
Serial No.:	09/884,523	Group Art Unit:	2143
Filed:	June 18, 2001	Docket:	7603.01
Title:	TRANSACTION PROCESSING SYSTEMS		

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

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By: 
Name: Kathleen KrochkoCommissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

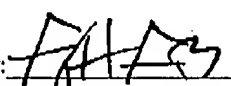
We are transmitting herewith the attached:

- ☒ Transmittal sheet, in duplicate, containing a Certificate of Mailing or Transmission under 37 CFR 1.8.
- ☒ Reply Brief of Appellants.

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers, if appropriate.

Please charge all fees to Deposit Account No. 14-0225 of NCR Corporation (the assignee of the present application). A duplicate of this paper is enclosed.

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NOV 03 2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:)	
Inventors: Michael G. Coutts et al.)	Examiner: Jerry B. Dennison
Serial #: 09/884,523)	Group Art Unit: 2143
Filed: June 18, 2001)	Appeal No.: _____
Title: <u>TRANSACTION PROCESSING SYSTEMS</u>)	

REPLY BRIEF OF APPELLANTS

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 C.F.R. §41.41, Appellants' attorney hereby submits the Reply Brief of Appellants in response to the Examiner's Answer dated September 3, 2008 for the above-identified application.

No fee is required for filing this supplemental Brief of Appellants. However, the Office is authorized to charge any necessary fees or credit any overpayments to Deposit Account No. 14-0225 of NCR Corporation, the assignee of the present invention.

I. ARGUMENTS

In the Answer, the Examiner essentially reiterates the prior rejections, albeit with additional remarks. In this regard, this Reply Brief of Appellants incorporates by reference herein the entirety of the previously filed Brief of Appellants.

The Examiner's additional remarks are set forth below:

(10) Response to Argument

Applicant presents the same argument for sections B-D:

1.) "that Vachon does not teach or suggest that each of the peripheral devices has an independent associated control application that communicates directly with each other independent of the central processor, whereby, in use, each peripheral device operates in response to signals generated by the central processor

as well as all other peripheral devices whose operation depends on or is connected with the state of that peripheral device" [Br. 5].

In response to Argument 1.) Examiner respectfully disagrees.

Vachon disclosed, "Transfer of data by peripheral devices via DMA without processor intervention, however, is especially suitable for computerized data acquisition applications" (Vachon, col. 1, lines 55-60).

Vachon also explicitly disclosed, "The interfacing device is also capable of transferring data between devices located on the peripheral bus as well as performing control functions for those devices requiring processor intervention" (Vachon, col. 2, lines 37-41).

These citations clearly show that the peripheral devices of Vachon communicate with each other without processor intervention.

The locations of Vachon cited by the Examiner's Answer are set forth below:

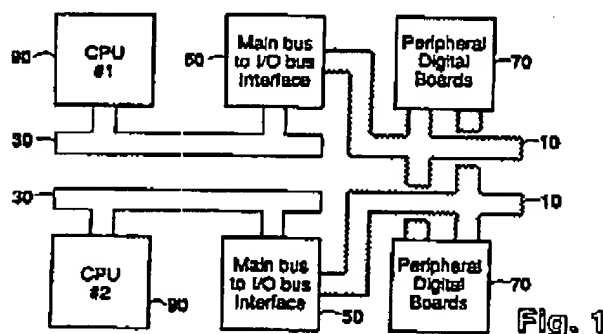
Vachon: Col. 1, lines 55-60

Transfer of data by peripheral devices via DMA without processor intervention, however, is especially suitable for computerized data acquisition applications.

Vachon: Col. 2, lines 37-41

The interfacing device is also capable of transferring data between devices located on the peripheral bus as well as performing control functions for those devices requiring processor intervention.

These portions of Vachon refer to the interfacing device 50 shown in FIG. 1:



Vachon: Col. 3, lines 16-35

FIG. 1 is a schematic representation of a computerized data acquisition system employing a peripheral I/O bus in accordance with the present invention. Owing to its simplicity, the peripheral I/O bus 10 is extensible so that peripheral data acquisition devices 70 which interface to it may be located physically distant from the rest of the system without performance degradation. The peripheral I/O

bus 10 is interfaced to the main processor bus 30 via a bus interfacing device 50. Connected to the main processor bus 30 is a main data acquisition processor 90 along with associated peripherals. In the particular embodiment shown, all of the components are made redundant with the two peripheral I/O buses directly interconnected.

The peripheral I/O bus 10 described herein is a **single-master/multiple-slave bus**. The peripheral I/O bus 10 is interfaced to the main processor bus 30 by an **intelligent bus interfacing device** used as a main bus to I/O bus interface and referred to herein as the **bus master 50**.

However, relevant descriptions can also be found at other locations of Vachon:

Vachon: Col. 2, lines 15-22

Further adding to processor overhead is the fact that the **data gathered from separate devices may be related**, requiring the processor to manipulate the gathered data in some fashion before it is in a useful form. For example, **two separate sources of data may need to interact**. Processor overhead would be reduced if the data interaction could take place before being input to the processor.

Vachon: Col. 2, lines 57-61

It is a further object of the present invention for the **programmable interfacing device to be capable of assuming control responsibilities for slave peripheral devices on the peripheral I/O bus and transferring data between them**.

Vachon: Col. 7, lines 34-38

Thus, using address register 71, data input register 73 and data output register 74, the **bus master is able to move data between devices located on the peripheral bus 10, as well as move data to and from the dual-ported RAM**.

Thus, the peripheral digital boards 70 of Vachon only operate under the control of signals generated by the interface device 50, which is the bus master. Yet, Vachon acknowledges that **data gathered from separate devices may be related**, and that **two separate sources of data (i.e., the peripheral digital boards 70) may need to interact**. However, it is the **interface device 50 that assumes control responsibilities for the slave peripheral devices 70 on the peripheral I/O bus 10 and transfers data between the slave peripheral devices 70**.

Appellants' independent claims, on the other hand, recite that **"each of the peripheral devices has an independent associated control application that communicates directly with each other independent of the central processor, whereby, in use, each peripheral device operates in response to signals generated by the central processor as well as all other peripheral devices whose operation depends on or is connected with the state of that peripheral device."**

The peripheral digital boards 70 of Vachon do not communicate directly with each other, and the peripheral digital boards 70 of Vachon do not operate in response to signals generated by other peripheral digital boards 70 of Vachon. Instead, the peripheral digital boards 70 of Vachon operate only in response to the interface device 50, i.e., the bus master.

Consequently, the cited references, taken in combination, fail to teach all the limitations of Appellants' claimed invention.

III. CONCLUSION

In light of the above arguments, Appellants' attorney respectfully submits that the cited references do not anticipate nor render obvious the claimed invention. More specifically, Appellant's claims recite novel physical features which patentably distinguish over any and all references under 35 U.S.C. §§ 102 and 103.

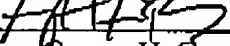
As a result, a decision by the Board of Patent Appeals and Interferences reversing the Examiner and directing allowance of the pending claims in the subject application is respectfully solicited.

Respectfully submitted,

GATES & COOPER LLP
Attorneys for Appellants

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Date: November 3, 2008

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